

REMARKS

Claims 1, 4-10, 13-17, and 20 are presently pending and stand rejected. Continued Examination is respectfully requested.

Claim 1, 9, and 17 were rejected under 35 U.S.C. 103(a) as being obvious from the combination of Jones in view of Gelsomini. Claim 20 was rejected as being obvious from the combination of Jones, Gelsomini, and Khoury.

Claim 1 recites, among other limitations, “determining if the state of the element is equal to an expected state using a verify circuit, wherein the state of the element is a state of the electrical resistance of the element”. Examiner has indicated that Jones discloses “determining if the state of the element is equal to an expected state (VERIFY DATA 0 in Fig. 3b) using a verify circuit (308 in Fig. 3a); and outputting a valid signal (FAST VERIFY OUTPUT of 390 in Fig. 3b) if the state of the element is equal to said expected state (if DR0 is equal to VERIFY DATA 0 in Fig. 3b;”. Examiner has also indicated that Gelsomini teaches “a thin oxide gated fuse ... wherein a state of the fuse is a state of the electrical resistance of the fuse (inherent as a fuse).” Examiner also indicated that “It would be obvious at the time the invention was made ... to substitute a thin oxide gated fuse ... as an equivalent memory element ... such that the state of the element is a state of the electrical resistance of the element”.

Assignee respectfully traverses the rejection and submits that even if Examiner is correct about the foregoing, the proposed combination does not teach “determining if the state of the element is equal to an expected state using a verify circuit, wherein the state of the element is a state of the electrical resistance of the element”. Examiner reads “verify circuit”, on “308 of Fig. 3a”, further illustrated in Fig. 3b showing exclusive OR (XOR) gate 380. Clearly the “308 of Fig. 3a” would not determine “the state of” the “thin oxide gate fuse” in the combination proposed by Examiner.

For the reasons above, Assignee respectfully submit that the combination of Jones, and Gelsomini do not teach or fairly suggest “wherein the state is a state of electrical resistance”. Accordingly, Examiner is requested to withdraw the rejection to claims 1, 9, 17, and 20 as well as to dependent claims 4-8, 10, and 13-16.

The pending claims were also rejected on the grounds of double patenting. A nonstatutory obviousness type double patenting rejection can be overcome by a timely

filed terminal disclaimer. Accordingly, Assignee presents Examiner with a terminal disclaimer and it is respectfully submitted that the foregoing rejection is now overcome.

For at least the foregoing reasons, each of the pending claims are in a condition for allowance. Please charge any required fees not paid herewith or credit any overpayment to the Deposit Account of McAndrews, Held & Malloy, Ltd., Account No. 13-0017. In view of the foregoing, it is respectfully submitted that the pending claims define allowable subject matter. Should anything remain in order to place the present application in condition for allowance, the Examiner is kindly invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,



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